

CLAIMS:

We claim:

- 1 1. A method of forming a microelectronic structure on a semiconductor material
2 having a silicon surface layer on a substrate, comprising the steps of:
3 a. implanting first dopant ions onto the surface layer;
4 b. subjecting the semiconductor material to a first annealing process; and
5 c. subjecting the semiconductor material to a second annealing process.
- 1 2. The method of claim 1, comprising the step of implanting second dopant ions of a
2 second conductivity type opposite in polarity to the first conductivity type onto the
3 surface layer, and wherein the step of implanting second dopant ions occurs:
4 a. at an acceleration energy from 50 eV to 5000 eV; and
5 b. with a dosage from $1 \times 10^{13}/\text{cm}^2$ to $1 \times 10^{16}/\text{cm}^2$.
- 1 3. The method of claim 1, wherein the step of implanting first dopant ions comprises
2 at least one high energy implantation step greater than 200keV, and at least one
3 low energy implantation step less than 5keV.
- 1 4. The method of claim 3, wherein the high-energy ion implantation step is carried
2 out:
3 a. at an energy level of about 200 keV to about 2000 keV; and
4 b. with a dosage from $1 \times 10^{13}/\text{cm}^2$ to $1 \times 10^{17}/\text{cm}^2$.
- 1 5. The method of claim 1, wherein the first annealing process comprises:
2 a. heating the semiconductor material from about 800°C to about 1200°C
3 with a ramp-up rate of about 50°C per second to about 1000°C per
4 second; and
5 b. after reaching a first desired temperature, holding the temperature for a
6 time period from about 1 millisecond to about 1000 seconds.

- 1 6. The method of claim 1, wherein the first annealing process includes a cooling
2 process that comprises cooling the semiconductor material at a ramp-down rate
3 from about 50°C per second to about 500°C per second.
- 1 7. The method of claim 1, wherein the second annealing process comprises heating
2 the semiconductor material at a temperature from about 400°C to about 650°C,
3 for a time period from about 1 second to about 10 hours.
- 1 8. The method of claim 1, wherein the second annealing process comprises heating
2 the semiconductor material with such temperature, amount of time, and heating
3 and cooling rates so that minimal dopant diffusion occurs.
- 1 9. The method of claim 1, wherein at least a part of the first and second annealing
2 processes occur in one selected from the group consisting of: a vacuum,
3 nitrogen gas, and inert gas.
- 1 10. The method of claim 2, wherein the second dopant ions are selected from the
2 group consisting of boron, arsenic, phosphorus, and antimony.
- 1 11. The method of claim 2 wherein the second dopant ions have a concentration of
2 about 1×10^{16} ions/cm³ to about 1×10^{21} ions/cm³.
- 1 12. The method of claim 1 wherein the second annealing process occurs any time
2 after the first annealing process.

- 1 13. A method of forming a microelectronic structure on a semiconductor material by
2 molecular beam epitaxy growth, comprising the steps of:
- 3 a. exposing, in a vacuum chamber, a single crystal semiconductor body to a
4 flux of one or more atomic or molecular species, with the body maintained
5 at a temperature greater than about 100°C and less than about 800°C;
- 6 b. depositing a single crystal epitaxial layer with doped atoms that are
7 electrically active; and
- 8 c. subjecting the semiconductor material to a post-growth annealing process.
- 1 14. The method of claim 13, wherein the annealing process occurs *in situ* in one
2 selected from the group consisting of: a vacuum, nitrogen gas, and inert gas.
- 1 15. The method of claim 13, wherein the annealing process comprises heating the
2 semiconductor material with such temperature, amount of time, and heating and
3 cooling rates so that minimal dopant diffusion occurs.